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FOR

METAL LOCAL INTERCONNECT SELF-ALIGNED SOURCE FLASH CELL

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METAL LOCAL INTERCONNECT SELF-ALIGNED SOURCE FLASH CELL

Field of the Invention

[0001] This invention relates to semiconductor fabrication processing and, more particularly, to a fabrication method for forming storage cells in semiconductor devices, such as non-volatile flash memory devices.

Background of the Invention

[0002] Non-volatile semiconductor memory devices are currently used extensively through the electronics industry. One type of non-volatile semiconductor memory devices employs the use of floating gate memory cells that are able to retain and transfer charge through a variety of mechanisms which include avalanche injection, channel injection, tunneling, etc. A flash memory device is such a semiconductor device that utilizes a floating gate memory cell. As is the case with most semiconductors being fabricated, the industry continues to push for smaller devices that contain a larger number of memory cells than each previous generation. This is also the case for the flash memory device.

[0003] In a flash memory device, fabrication of the components that make up the floating gate transistor determines the ability of the device to be programmed and retain an electrical charge as well as the ability of the device to be reprogrammed by being erased (or the removal of the electrical charge). Flash memory cells comprising floating gate transistors are laid out in such a manner that a plurality of cells forms a memory array.

[0004] A device in the programmed state, i.e., charge stored on the floating gate, represents a stored "0" and a device in the non-programmed state, i.e., no charge stored on the floating gate, represents a stored "1." Reading a device in the programmed state will cause the device to conduct heavily, while reading a device in the non-programmed state the device will not conduct. Each

floating gate transistor in the array has a common source line and the common source line requires sophisticated fabrication techniques.

[0005] The present invention provides a floating gate device structure and method to fabricate a low resistant local interconnect self-aligned source that will provide enhanced operation of a flash memory cell device.

Summary of the Invention

[0006] Exemplary implementations of the present invention comprise a flash memory device and processes therefor.

[0007] A first exemplary implementation of the present invention includes a flash memory device comprising a series of floating gate devices each having an implanted source electrode self-aligned to a respective gate electrode, the implanted source electrodes connected together by a conductively doped active area, and a metal interconnect running a major length of source electrodes that are serially connect by the self-aligned source, the metal interconnect making substantially continuous contact therebetween. The metal interconnect may comprise a tungsten-based metal, such as tungsten or tungsten/titanium.

[0008] A second exemplary implementation of the present invention includes process steps for forming a flash memory device on a semiconductor assembly.

[0009] A series of floating gate devices having their source electrodes connected together by a conductively doped active area is formed. The source electrodes of each device are self-aligned to their respective transistor gates of each said floating gate device. Then a nitride barrier layer is formed such that it overlies each transistor gate. Next, a planarized insulation layer is formed over said nitride barrier layer. Portions of the planarized insulation layer are removed while using the nitride barrier layer to self-align an interconnect via to underlying source electrodes. The nitride barrier layer is etched away, such as with an anisotropic dry etch, to

expose the underlying self-aligned sources. A metal local interconnect is formed into the interconnect via. The metal interconnect runs the major length of the source electrodes, while making contact therebetween. It is optional to simultaneously form metal drain plugs for each floating gate device and self-aligning each metal drain plug to an underlying drain electrode. The metal interconnect and the metal drain plug may be formed from a tungsten-based metal, such as tungsten or tungsten/titanium.

Brief Description of the Drawings

[0010] Figure 1 is a top-down view depicting the layout of an array of flash cells, each cell utilizing a tungsten local interconnect- self aligned source (WLI-SAS flash cell).

[0011] Figure 2 is a cross-sectional view taken through line 1-1' of Figure 1 after the definition of active areas and shallow trench isolation.

[0012] Figure 3 is a cross-sectional view taken through line 2-2' of Figure 1 after the formation of a transistor gate stack for a floating gate device.

[0013] Figure 4 is a cross-sectional view following the cross-sectional view of Figure 2 taken after the removal of the shallow trench isolation oxide followed by a source implant and a blanket phosphorous and/or arsenic source/drain implant.

[0014] Figure 5 is a cross-sectional view following the cross-sectional view of Figure 3 taken after a phosphorous and/or arsenic source/drain implant.

[0015] Figure 6 is a cross-sectional view following the cross-sectional view of Figure 5 taken after the formation of transistor gate cap and spacers, followed by the deposition of a conformal layer of nitride and the formation of a planarized borophosphosilicate glass (BPSG) isolation layer.

[0016] Figure 7 is a cross-sectional view following the cross-sectional view of Figure 6 taken after the patterning and etching of contact via opening to expose the source and drain of the floating gate device.

[0017] Figure 8 is a cross-sectional view following the cross-sectional view of Figure 7 taken after the formation of a planarized layer of tungsten to create drain contact plugs and to create a tungsten local interconnect between each source.

[0018] Figure 9 is a cross-sectional view following the cross-sectional view of Figure 8 taken after the formation of a planarized layer of inner layer dielectric material that is patterned and etched to provide via openings to expose the drain contact plugs which is followed by the formation of a planarized metal to make interconnect between the drain plugs.

[0019] Figure 10 is a cross-sectional view following the cross-sectional view of Figure 5 taken after the formation of a planarized layer of tungsten to create a tungsten local interconnect between each source.

Detailed Description of the Invention

[0020] Exemplary implementations of the present invention directed to processes for fabricating a floating gate memory device are depicted in Figures 1-10.

[0021] Referring now to the top-down view of Figure 1, the layout of a WLI-SAS flash cell on wafer substrate 10 is presented. Active areas 21 define the location of source, drain and channel of the floating gate devices to be formed. Shallow trench isolation 23 provides isolation between neighboring gate devices. Wordlines 34 run horizontally and overlie the floating gates 32. Floating gates 32 span between self-aligned sources and drains that reside in the confines of active areas 21. Self-aligned drain contacts 82 make contact to underlying drains 51 and tungsten local interconnects 83 make contact to underlying self-aligned sources 41.

[0022] Figure 2 is a cross-sectional view of Figure 1 taken through line 1-1'. Referring now to Figure 2, future source/drain regions 21 are defined, followed by the formation of shallow trench isolation. The shallow trench isolation is formed first by etching trenches 22 into substrate 10. Trenches 22 are then filled with oxide 23 that is then planarized.

[0023] Figure 3 is a cross-sectional view of Figure 1 taken through line 2-21'. Referring now to Figure 3, various materials have been deposited and etched to form the transistor gate for each floating gate device. The transistor gate comprises tunnel oxide 31, a self-aligned floating gate 32, an inter-polysilicon dielectric (such as an oxide/nitride/oxide stack) 33, polysilicon wordline 34, which is typically capped with tungsten silicide 35 and dielectric cap 36, such as oxide or nitride. Figure 3 also shows the locations of future source/drain regions 21.

[0024] Figure 4 follows the view of Figure 2, while Figure 5 follows the view of Figure 3. Referring now to Figure 4, an etch is performed to remove shallow trench isolation oxide 23. Referring now to both Figures 4 and 5, photoresist 50 is patterned to expose a predetermined source region. Using photoresist as a mask, a source implant, typically using phosphorous and/or arsenic is performed to create self-aligned source region 41 (shown in both Figures 4 and 5). This source implant creates a source region that directly aligns itself to the transistor gate, thus the term self-aligned source. Next, photoresist 50 is stripped and a blanket source/drain implant (typically arsenic) is performed to form a deeper implanted self-aligned source region 41 and to form drain regions 51.

[0025] Figure 6 follows the view of Figure 5. Referring now to Figure 6, transistor isolation spacers 62 are formed. The conventional floating gate process uses oxide to form spacers 62. In the present invention, nitride is used in order to take advantage of the better dielectric qualities nitride possesses compared to oxide. Even though nitride is known to exert more stress than will oxide on underlying structures and possibly cause electrical changes, nitride is an effective etch stop material to use during the subsequently performed self-aligned contact etch. Regardless if oxide or nitride is used to spacers 62, following the formation of spacers 62, a conformal nitride etch stop barrier layer 63 is deposited which will cover source/drain regions 41 and 51 as well as

cap 61 and spacers 62. Then the structure is covered with the formation of BPSG material 64 that is planarized.

[0026] Referring now to Figure 7, BPSG material 64 is patterned with photoresist 71 to allow for a subsequent via etch (also defined as the self-aligned source contact etch or SAS etch) to form drain contact via openings 72 and source line opening 73. The via etch removes exposed BPSG material 64 and stops on etch stop barrier layer 63. Next, an etch is performed to clear the conformal nitride from the surface of source/drain regions 41 and 51.

[0027] Referring now to Figure 8, photoresist 71 (seen in Figure 7) is stripped and a conformal titanium nitride barrier layer 81 is deposited along the edges of via openings 72 and 73. Next, a metal such as tungsten-based metal (solely tungsten or titanium tungsten) is formed to fill drain contact via openings 72 and source line opening 73. The metal is then planarized to form self-aligned drain contacts 82 (or plugs 82) and local interconnect 83 that is self-aligned to source 41. Drain contact plugs 82 will subsequently become connected between the drain of selected floating gate devices and a digit line.

[0028] Referring now to Figure 9, an inner layer dielectric material 91 is formed over the present structure of Figure 8. Dielectric material 91 is planarized and then patterned and etched to form via openings 92 that expose underlying drain contact plugs 81. Next a metal 93 is formed that fills via openings 92. Metal 93 is planarized and serves as a digit line for the selected floating gate devices.

[0029] Figure 10 is a cross-sectional view taken along the self-aligned source. Referring now to Figure 10, local interconnect 82 makes connection to each source of a series of devices that are inner-connected by the self-aligned source implant. An important element of the present invention is the combination of metal local interconnect 83 (not seen in Figure 10), with the self-aligned source 41, in conjunction with self-aligned drain contacts 82 that significantly lowers source resistance and also allows the fabrication of a smaller floating gate device. The self-aligned source allows for a smaller cell simply by its inherent nature of being self-aligned to the transistor

gate of each floating gate device. The lowered source resistance, due to the presence of the metal local interconnect, gives better cell performance uniformity when comparing the performance of a cell that is relatively close to a source contact versus a cell fairly far away from a source contact. With the metal local interconnect, the overall size of the array can be reduced, as fewer source contacts will be needed compared to a conventional flash cell array. Most importantly, the metal local interconnect 83 connecting from source to source of series of devices will significantly reduce source resistance as the metal (such as a tungsten-based metal) provides a much better conducting line than does the conductively doped active area that forms the source for each device.

[0030] As demonstrated by the teachings of the present invention, the addition of the tungsten local interconnect to the self-aligned source electrode can be efficiently incorporated into conventional flash memory device fabrication methods.

[0031] It is to be understood that although the present invention has been described with reference to several preferred embodiments, various modifications, known to those skilled in the art, may be made to the process steps presented herein without departing from the invention as recited in the several claims appended hereto.